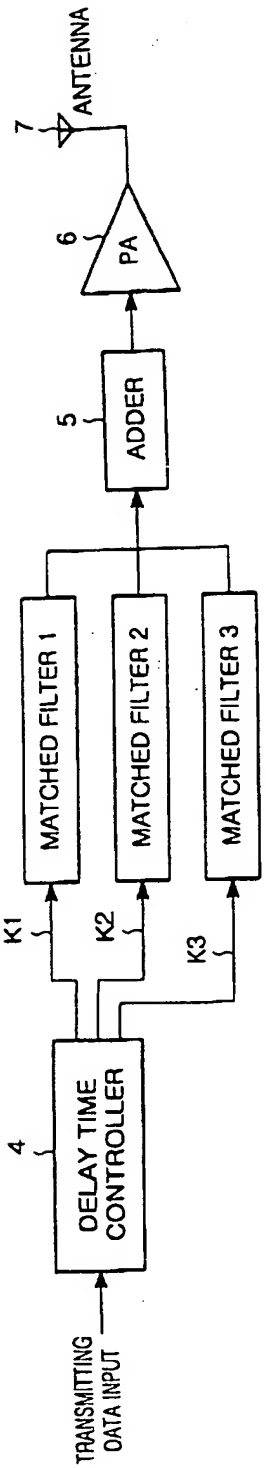
TRANSMITTING DATA INPUT
4
DELAY TIME CONTROLLER
K1
K2
K3
MATCHED FILTER 1
MATCHED FILTER 2
MATCHED FILTER 3
5
ADDER
6
PA
7
ANTENNA

FIG.1

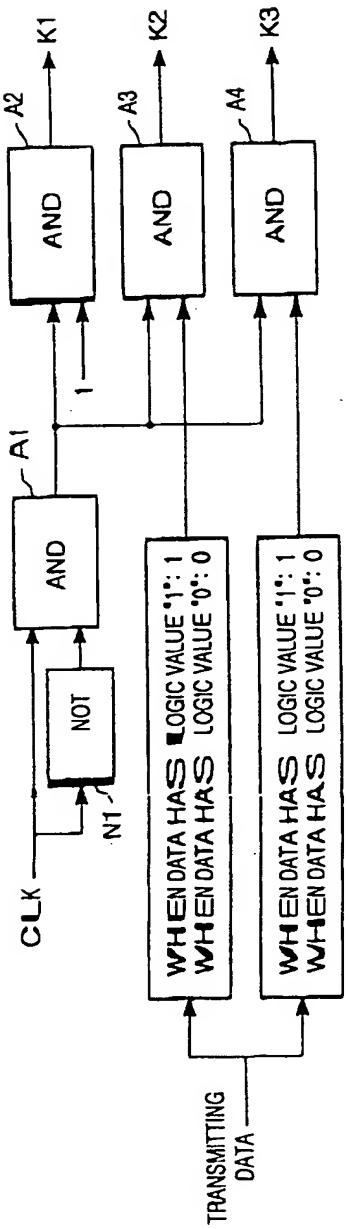
CLK
N1
NOT
AND
A1
1
AND
A2
K1
AND
A3
K2
AND
A4
K3
WHEN DATA HAS LOGIC VALUE "1": 1
WHEN DATA HAS LOGIC VALUE "0": 0
WHEN DATA HAS LOGIC VALUE "1": 1
WHEN DATA HAS LOGIC VALUE "0": 0
TRANSMITTING DATA

FIG. 2

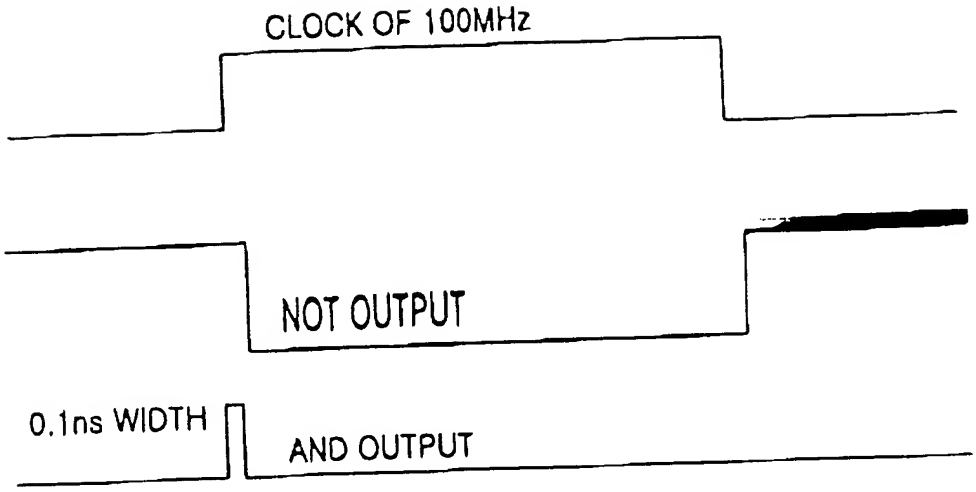

FIG.3

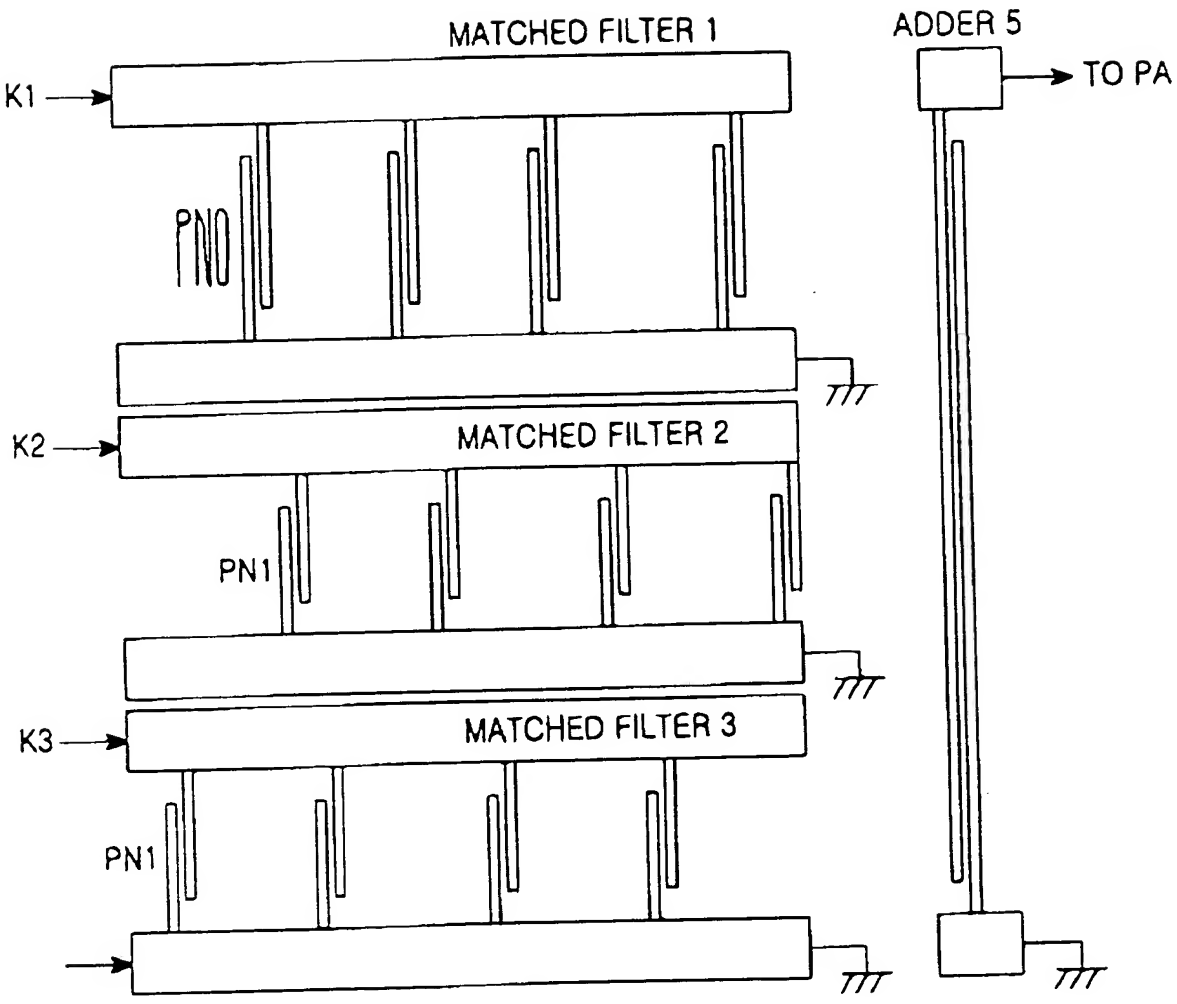
MATCHED FILTER 1
ADDER 5
TO PA
K1
PN0
K2
MATCHED FILTER 2
PN1
K3
MATCHED FILTER 3
PN1

FIG.4

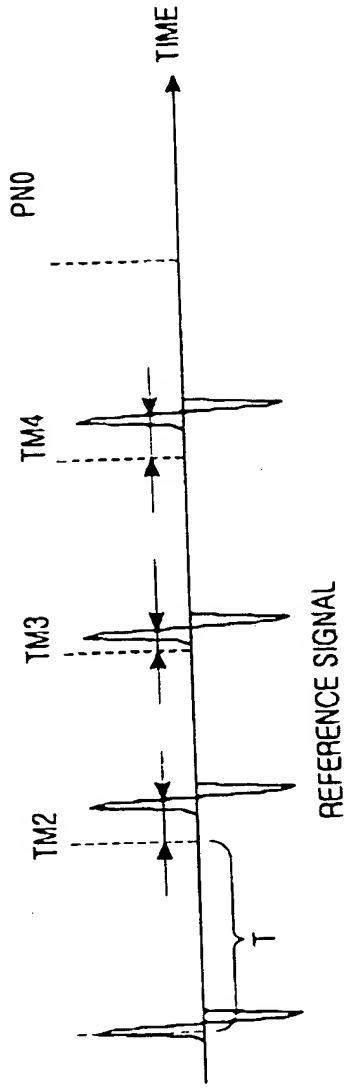

FIG.5

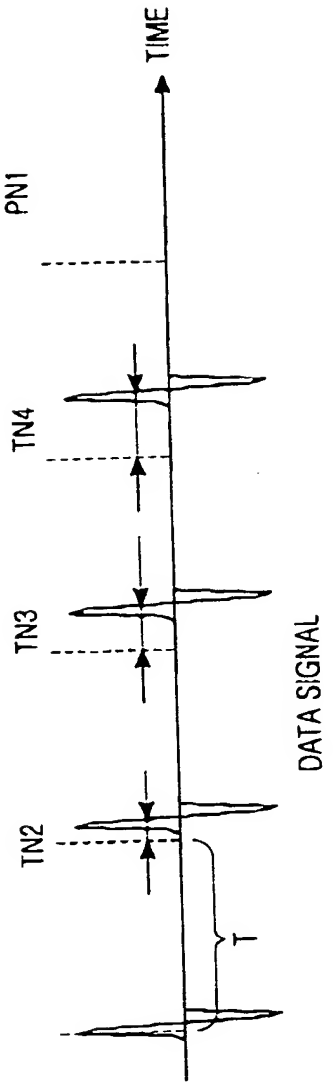

FIG.6

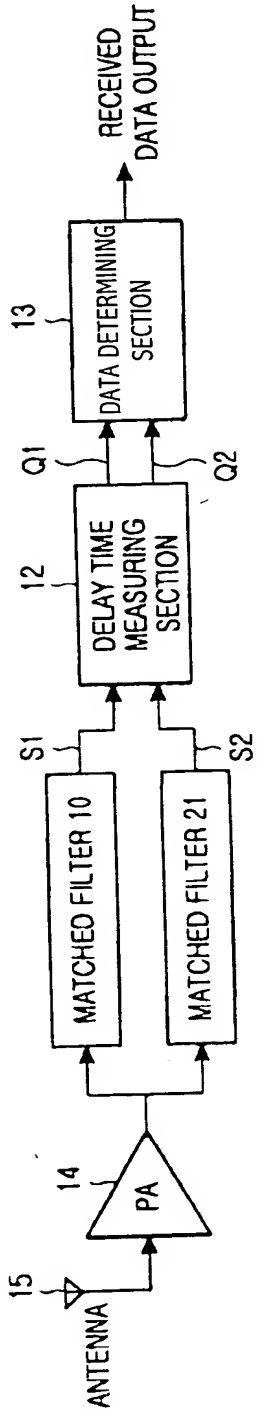
RECEIVED DATA OUTPUT
13
DATA DETERMINING SECTION
Q1
Q2
12
DELAY TIME MEASURING SECTION
S1
S2
MATCHED FILTER 10
MATCHED FILTER 21
14
PA
15
ANTENNA

FIG.7

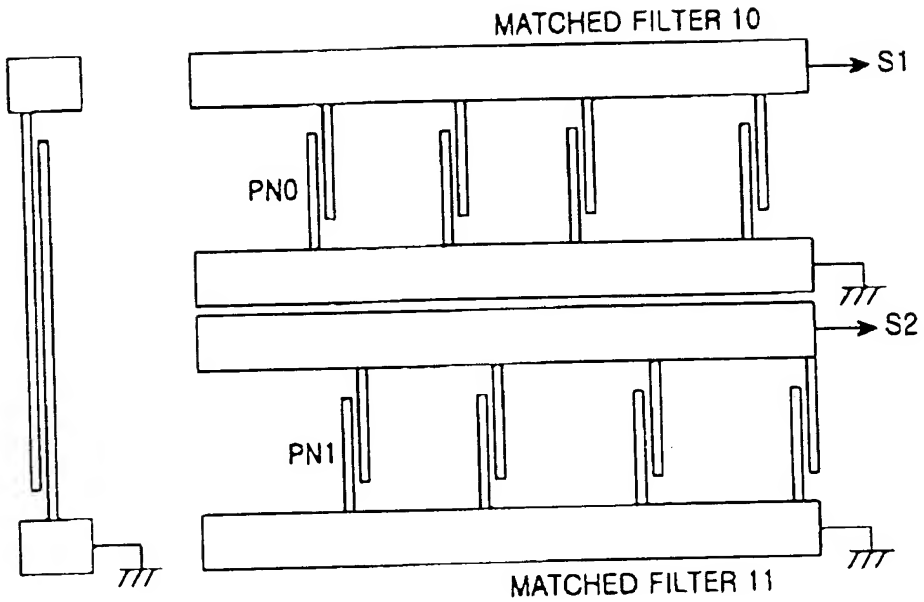

FIG.8

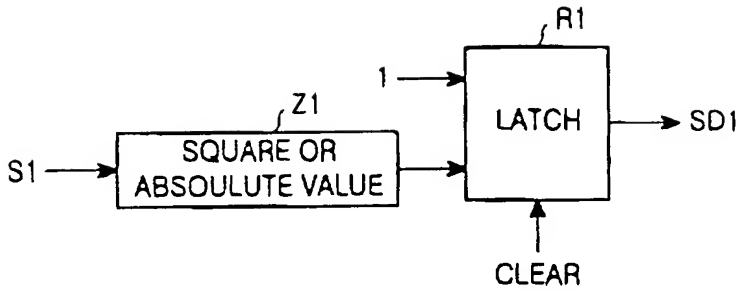
R1
1
Z1
LATCH
SD1
S1
SQUARE OR
ABSOULUTE VALUE
CLEAR

FIG.9

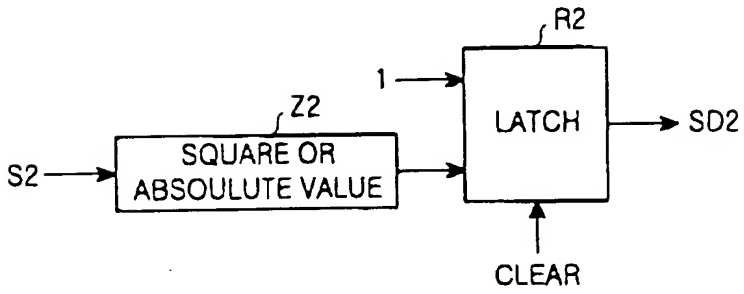
R2
1
Z2
LATCH
SD2
S2
SQUARE OR
ABSOULUTE VALUE
CLEAR

FIG.10

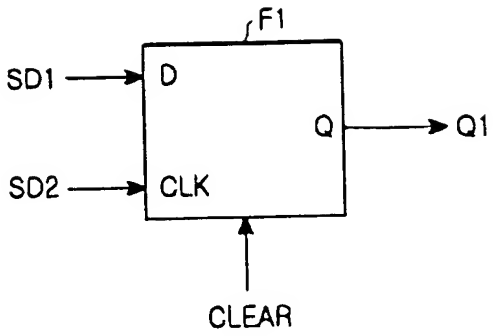

FIG.11

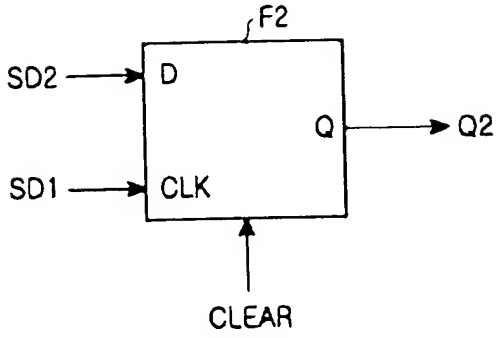

FIG.12

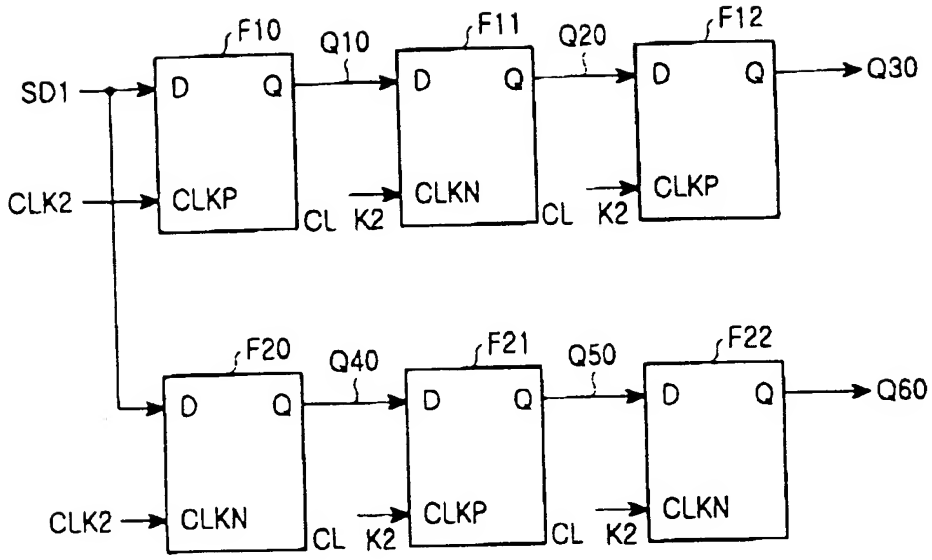
F10
Q10
F11
Q20
F12
SD1
D
Q
D
Q
D
Q
Q30
CLK2
CLKP
CL
K2
CLKN
CL
K2
CLKP
F20
Q40
F21
Q50
F22
D
Q
D
Q
D
Q
Q60
CLK2
CLKN
CL
K2
CLKP
CL
K2
CLKN

FIG.13

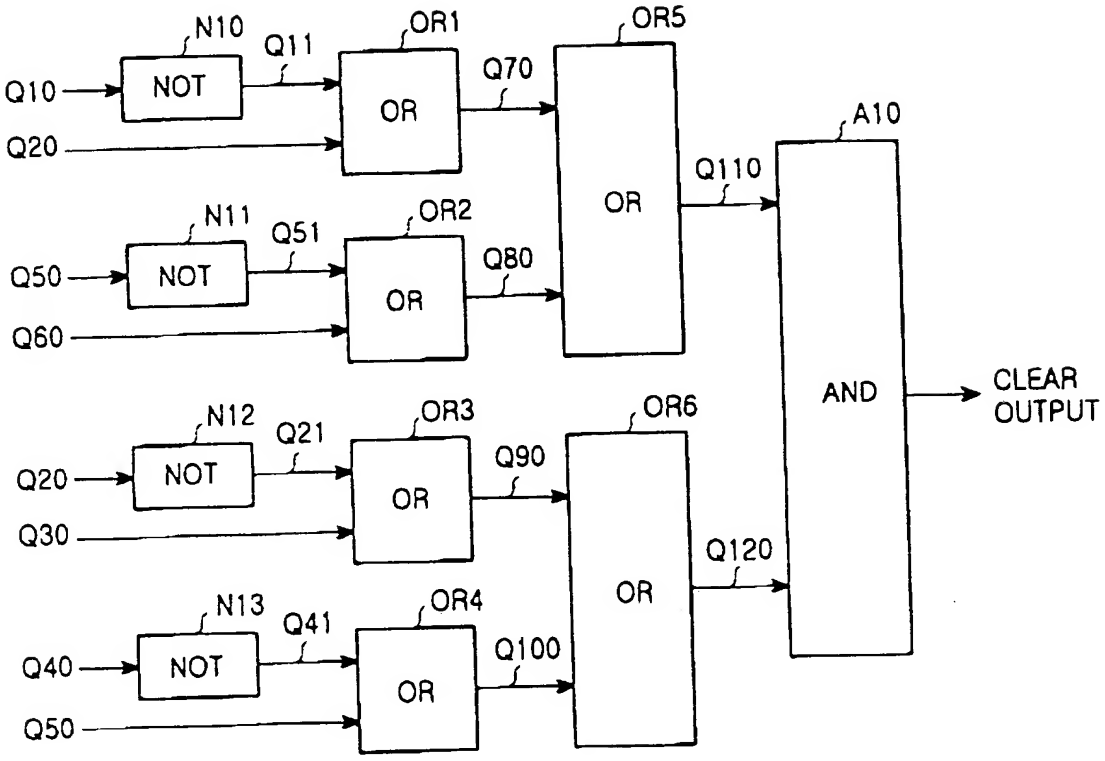
N10
Q11
OR1
Q70
OR5
A10
Q10
NOT
OR
Q20
Q110
N11
Q51
OR2
Q80
Q50
NOT
OR
AND
CLEAR
OUTPUT
Q60
N12
Q21
OR3
Q90
OR6
Q20
NOT
OR
Q30
Q120
N13
Q41
OR4
Q100
Q40
NOT
OR
Q50

FIG.14

Q1	Q2	DATA
0	0	X
0	1	1
1	0	0
1	1	X

FIG.15

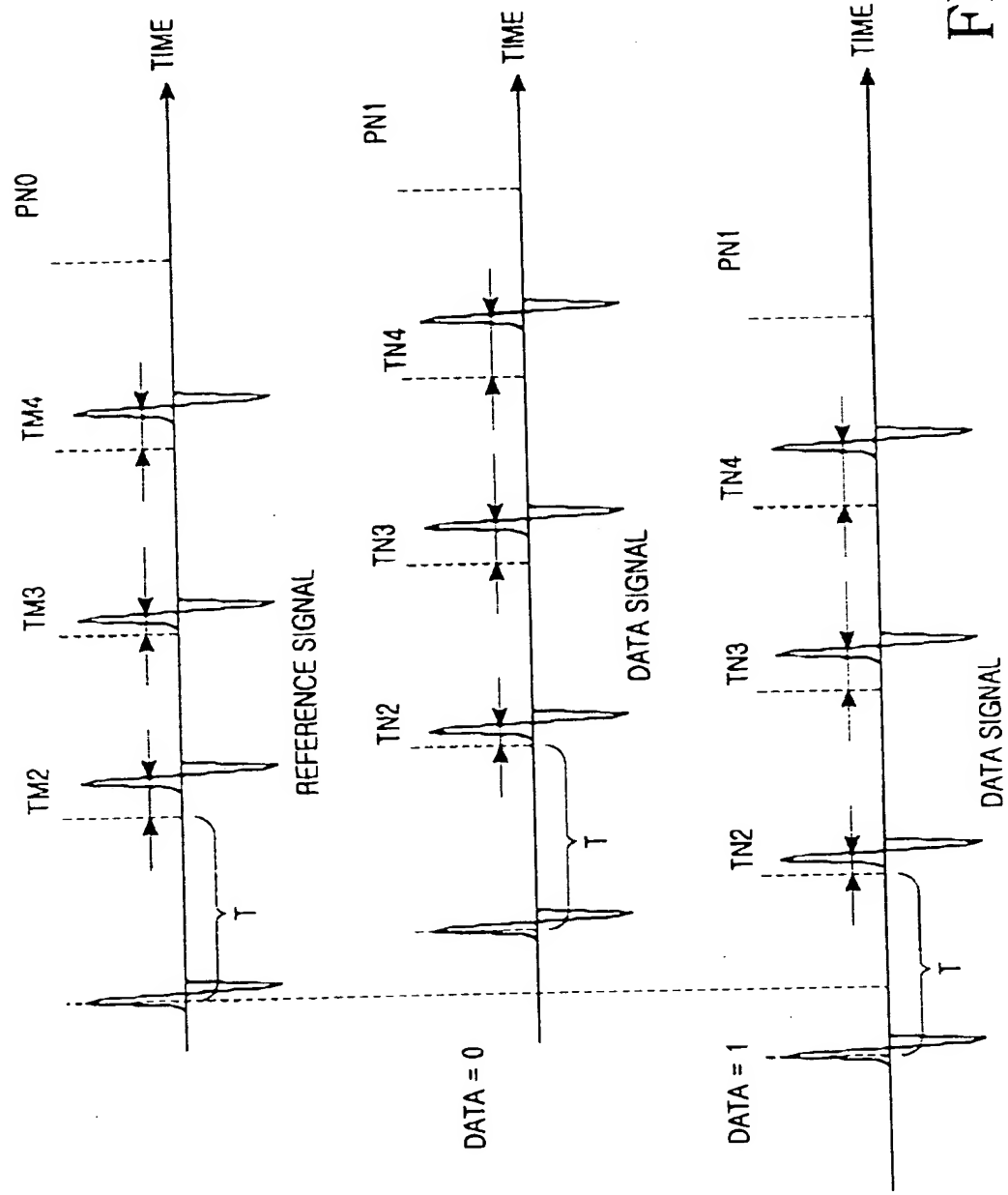
PN0
TIME
TM4
TM3
TM2
T
REFERENCE SIGNAL
DATA = 0
PN1
TIME
TN4
TN3
TN2
T
DATA SIGNAL
DATA = 1
PN1
TIME
TN4
TN3
TN2
T
DATA SIGNAL

FIG.16

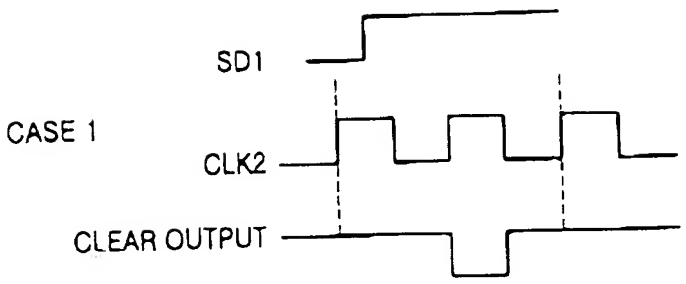

FIG.17

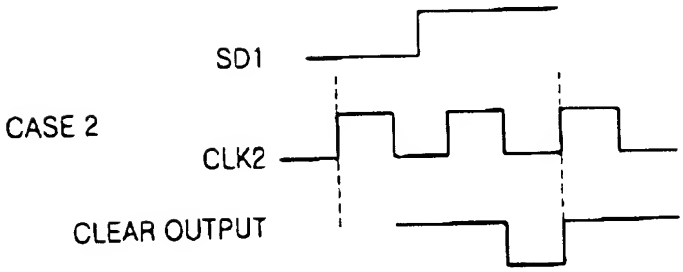

FIG.18

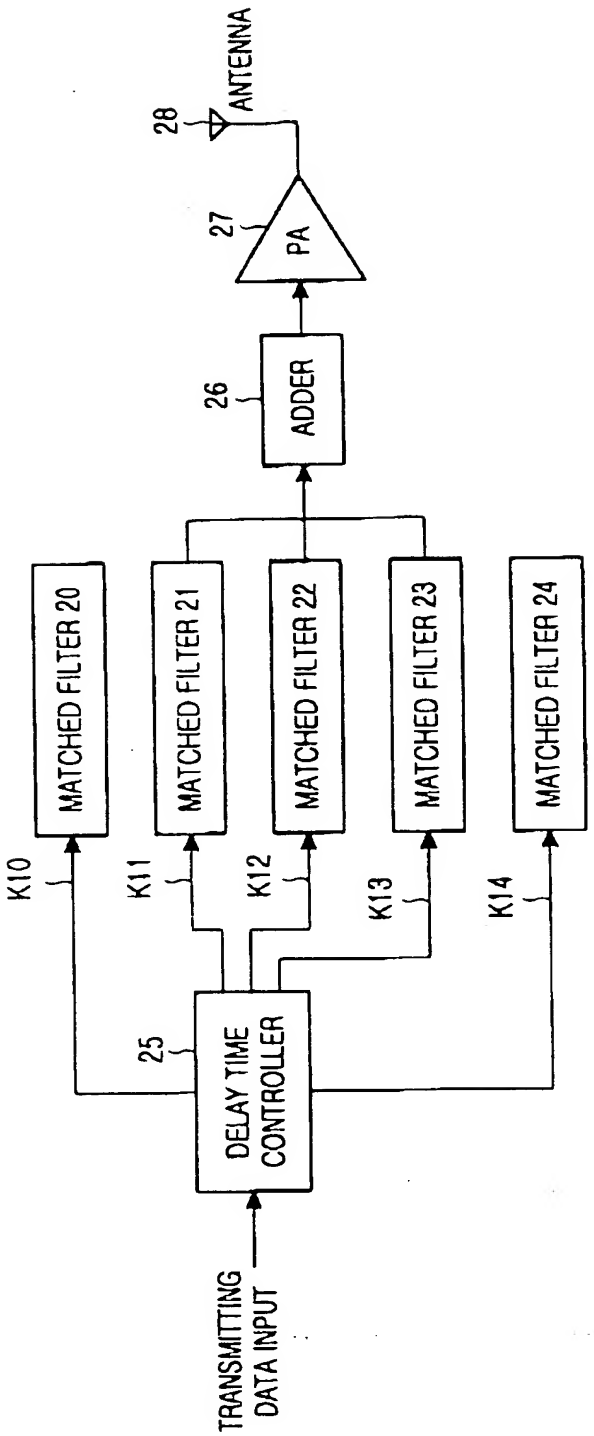
TRANSMITTING DATA INPUT
25
DELAY TIME CONTROLLER
K10
K11
K12
K13
K14
MATCHED FILTER 20
MATCHED FILTER 21
MATCHED FILTER 22
MATCHED FILTER 23
MATCHED FILTER 24
26
ADDER
27
PA
28
ANTENNA

FIG.19

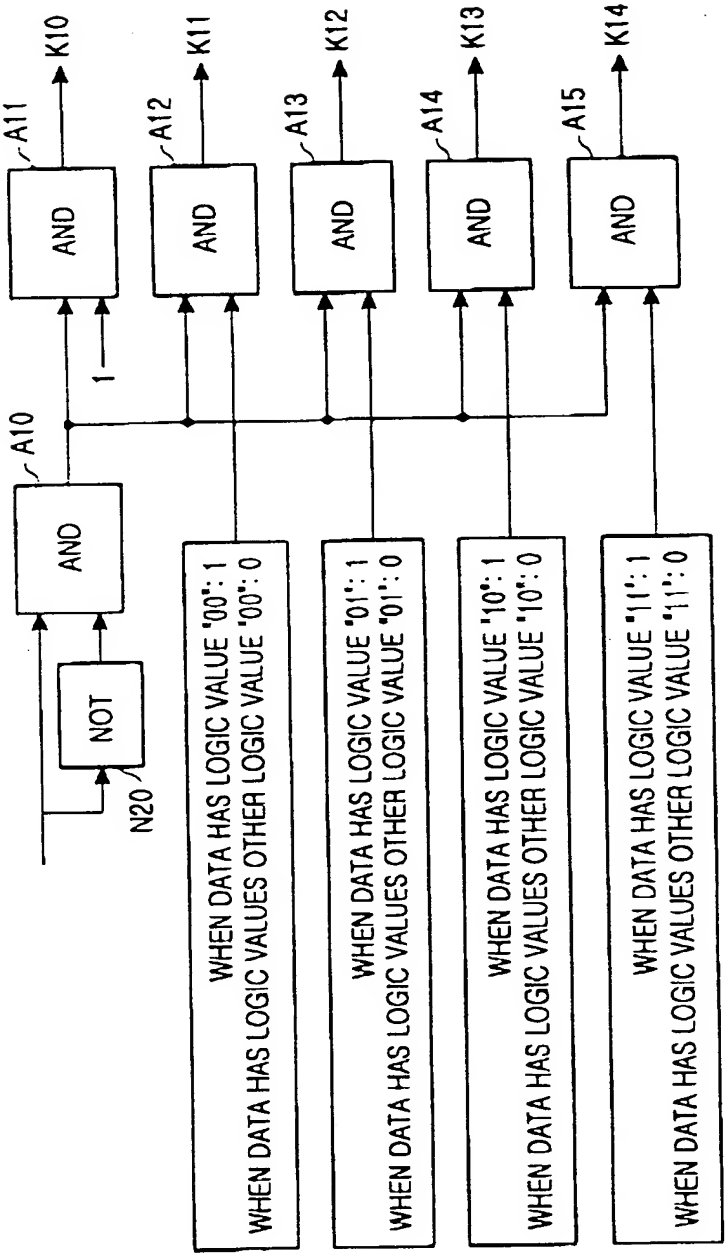
NOT
N20
AND
A10
1
AND
A11
K10
AND
A12
K11
AND
A13
K12
AND
A14
K13
AND
A15
K14
WHEN DATA HAS LOGIC VALUE "00": 1
WHEN DATA HAS LOGIC VALUES OTHER LOGIC VALUE "00": 0
WHEN DATA HAS LOGIC VALUE "01": 1
WHEN DATA HAS LOGIC VALUES OTHER LOGIC VALUE "01": 0
WHEN DATA HAS LOGIC VALUE "10": 1
WHEN DATA HAS LOGIC VALUES OTHER LOGIC VALUE "10": 0
WHEN DATA HAS LOGIC VALUE "11": 1
WHEN DATA HAS LOGIC VALUES OTHER LOGIC VALUE "11": 0

FIG.20

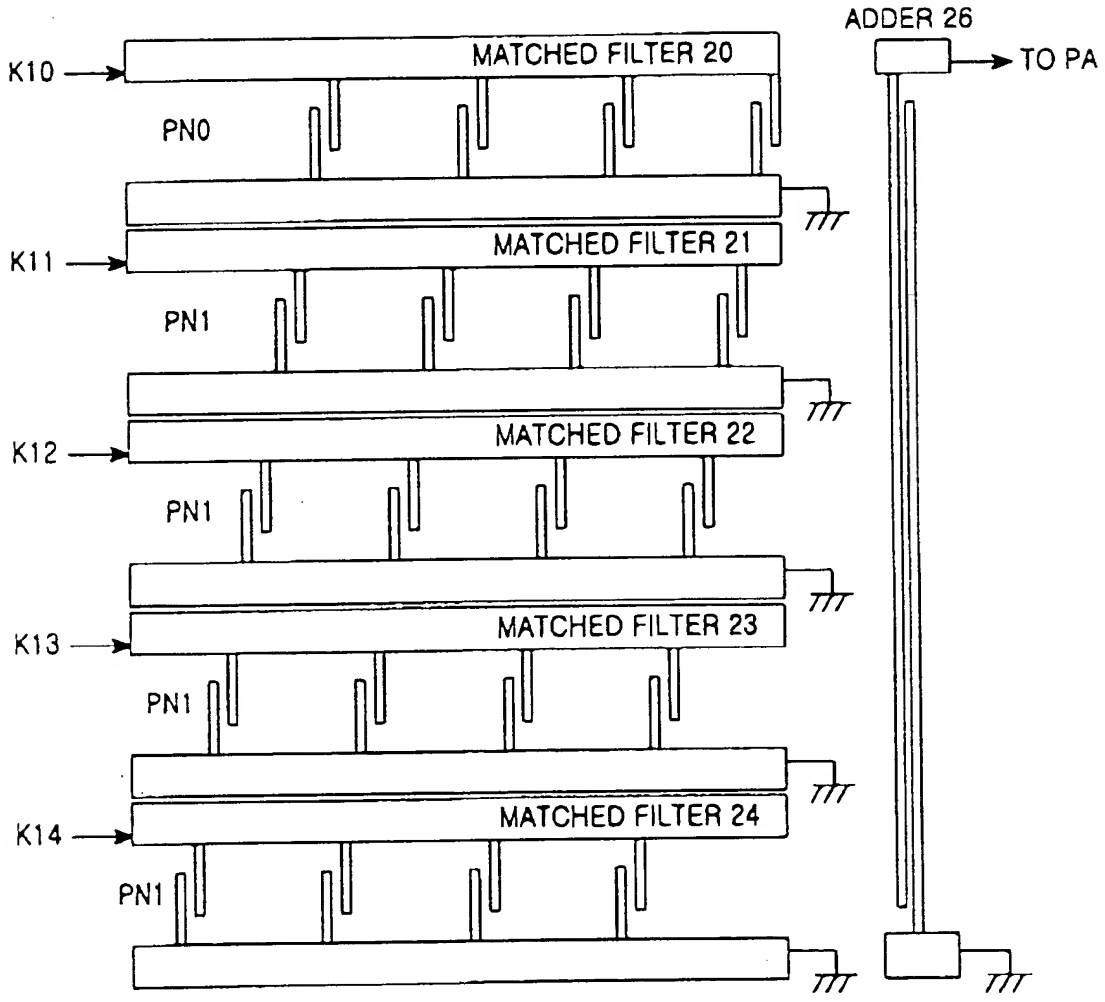
ADDER 26
TO PA
K10
MATCHED FILTER 20
PN0
K11
MATCHED FILTER 21
PN1
K12
MATCHED FILTER 22
PN1
K13
MATCHED FILTER 23
PN1
K14
MATCHED FILTER 24
PN1

FIG.21

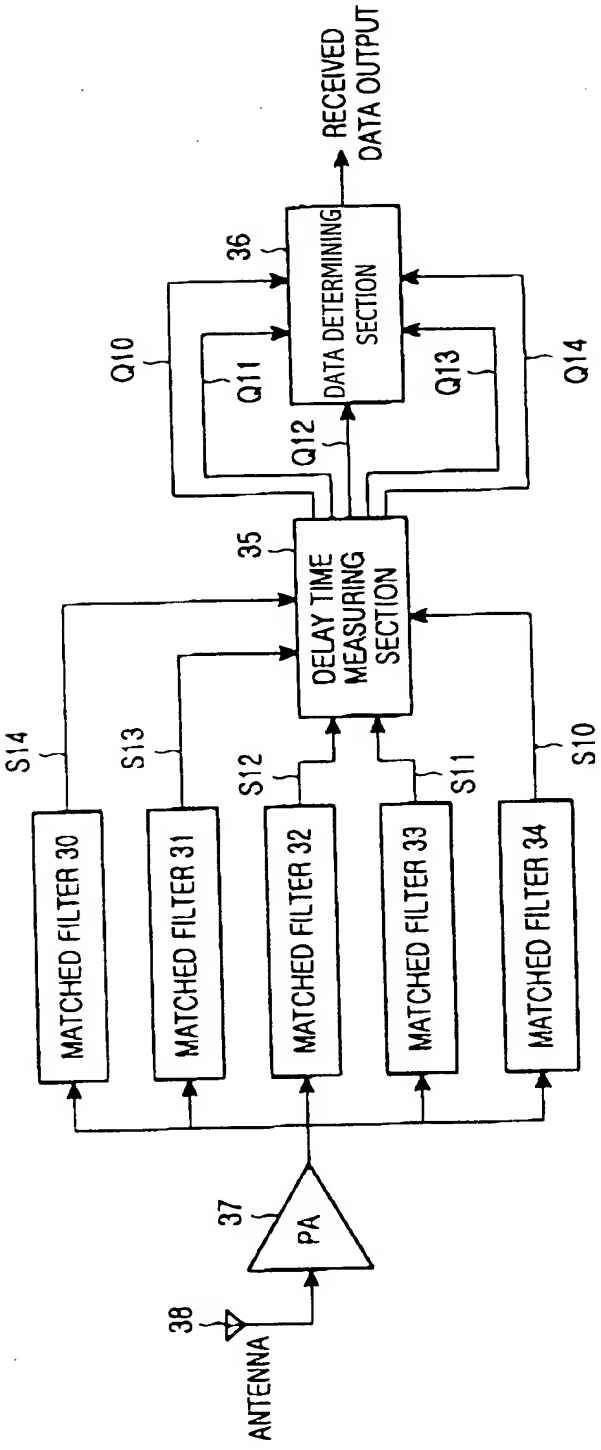
RECEIVED DATA OUTPUT
36
DATA DETERMINING SECTION
Q10
Q11
Q12
Q13
Q14
35
DELAY TIME MEASURING SECTION
S14
S13
S12
S11
S10
MATCHED FILTER 30
MATCHED FILTER 31
MATCHED FILTER 32
MATCHED FILTER 33
MATCHED FILTER 34
37
PA
38
ANTENNA

FIG.22

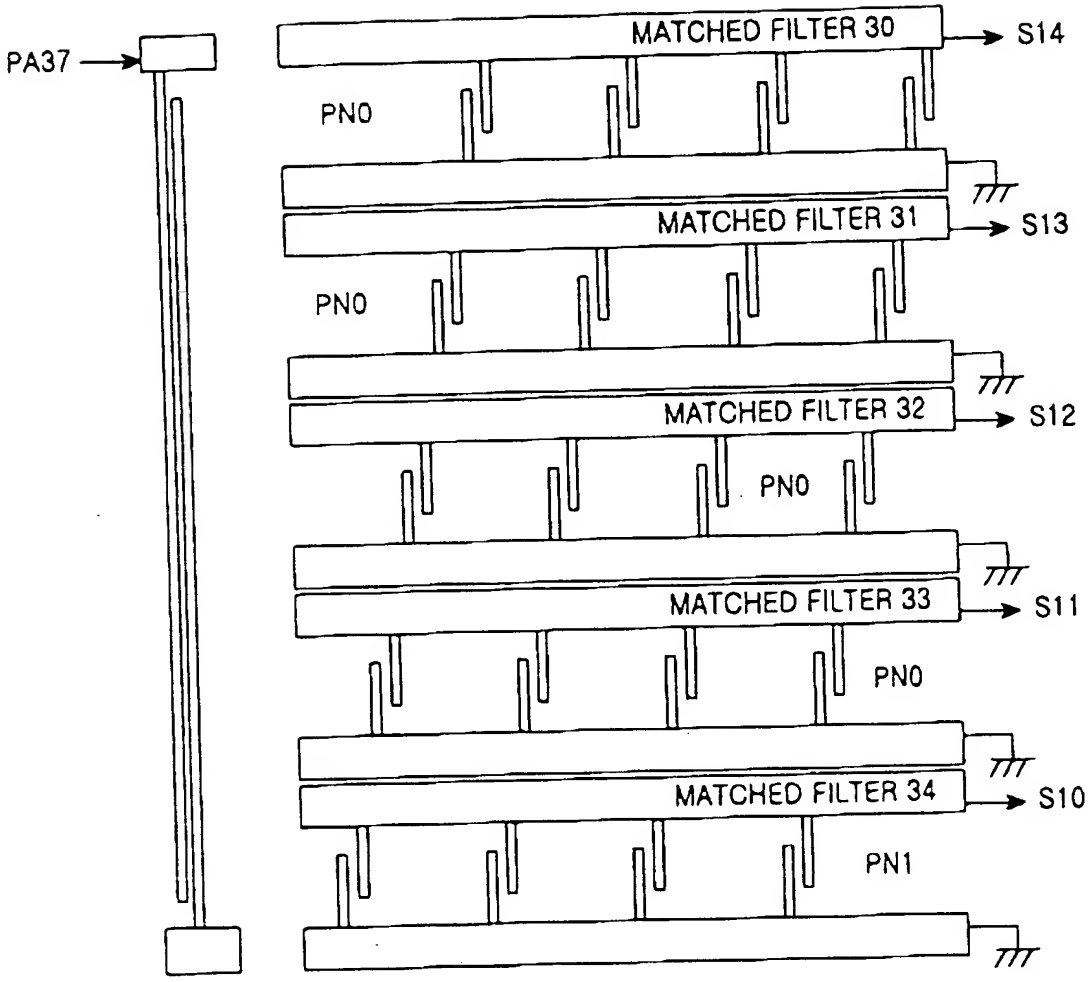
PA37
MATCHED FILTER 30
S14
PN0
MATCHED FILTER 31
S13
PN0
MATCHED FILTER 32
S12
PN0
MATCHED FILTER 33
S11
PN0
MATCHED FILTER 34
S10
PN1

FIG.23

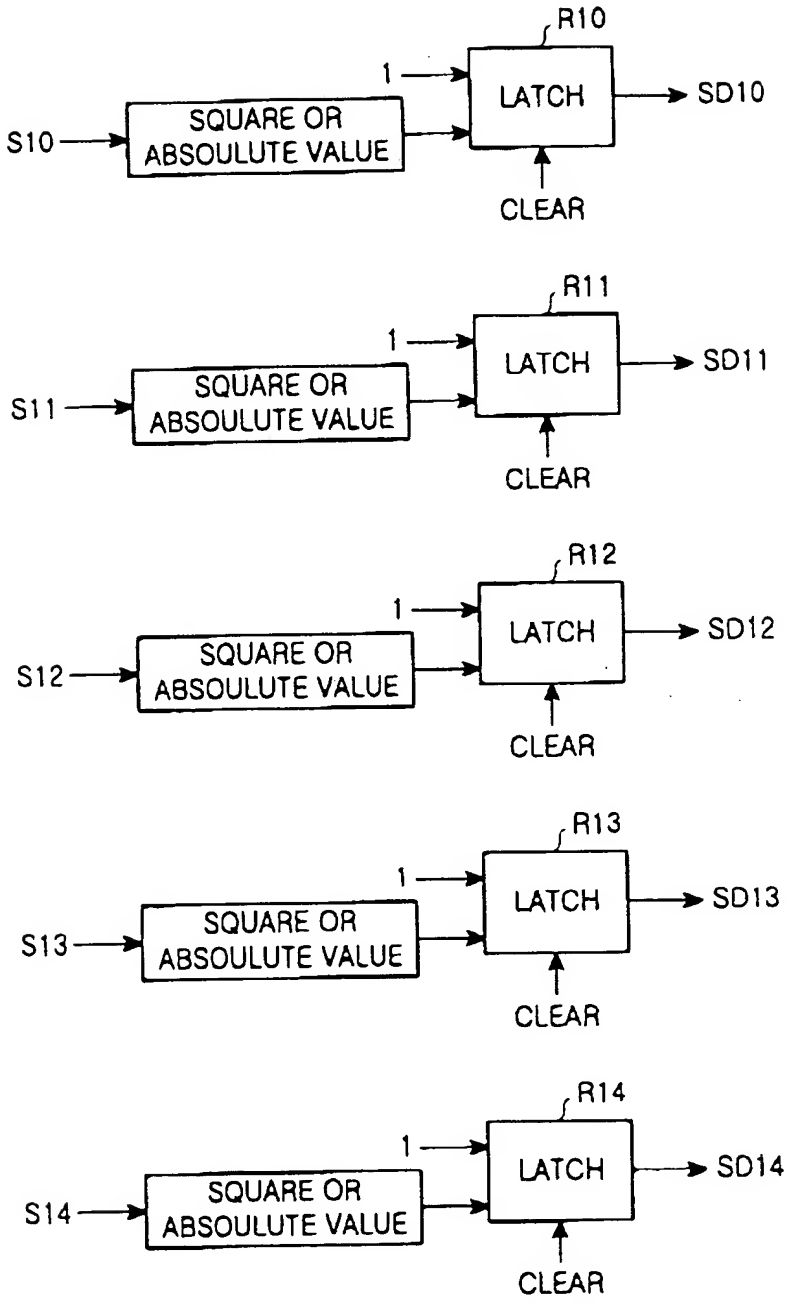
R10
1
LATCH
SD10
S10
SQUARE OR ABSOULUTE VALUE
CLEAR
R11
1
LATCH
SD11
S11
SQUARE OR ABSOULUTE VALUE
CLEAR
R12
1
LATCH
SD12
S12
SQUARE OR ABSOULUTE VALUE
CLEAR
R13
1
LATCH
SD13
S13
SQUARE OR ABSOULUTE VALUE
CLEAR
R14
1
LATCH
SD14
S14
SQUARE OR ABSOULUTE VALUE
CLEAR

FIG.24

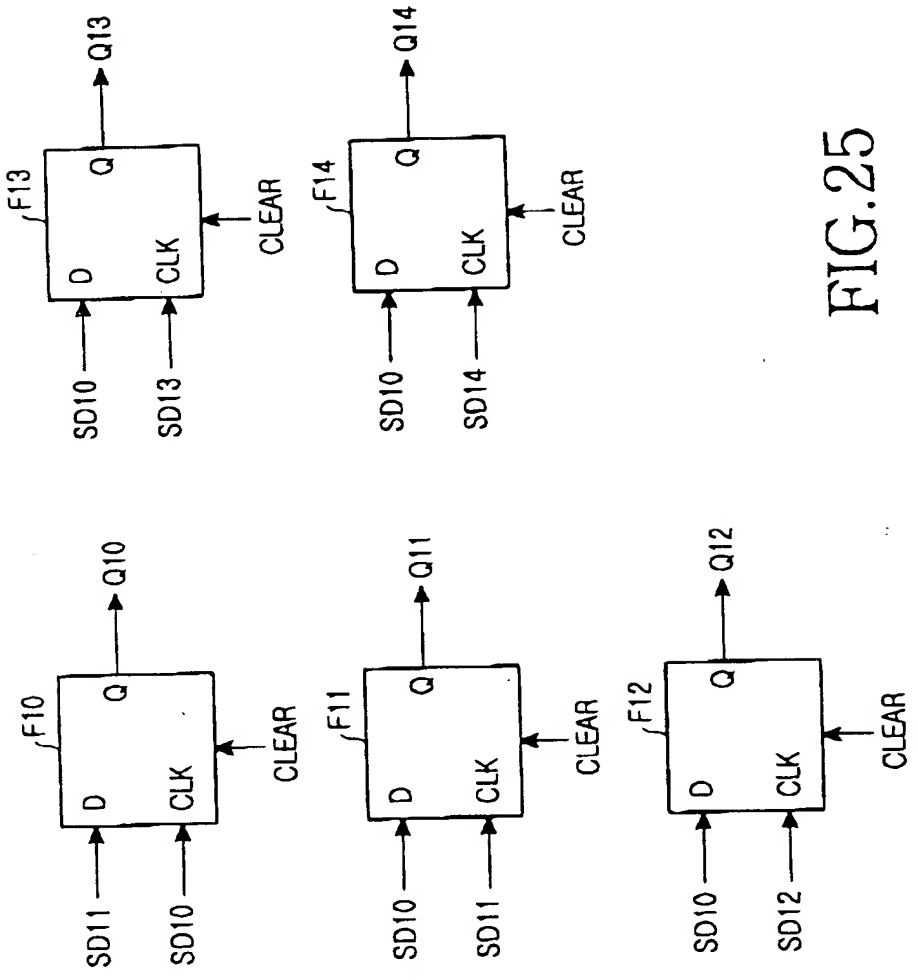
F13
Q13
Q
D
CLK
CLEAR
SD10
SD13
F14
Q14
Q
D
CLK
CLEAR
SD10
SD14
F10
Q10
Q
D
CLK
CLEAR
SD11
SD10
F11
Q11
Q
D
CLK
CLEAR
SD10
SD11
F12
Q12
Q
D
CLK
CLEAR
SD10
SD12

FIG.25

Q10	Q11	Q12	Q13	Q14	DATA
1	0	1	1	1	0,0
1	0	0	1	1	0,1
1	0	0	0	1	1,1
1	0	0	0	0	1,1

FIG.26

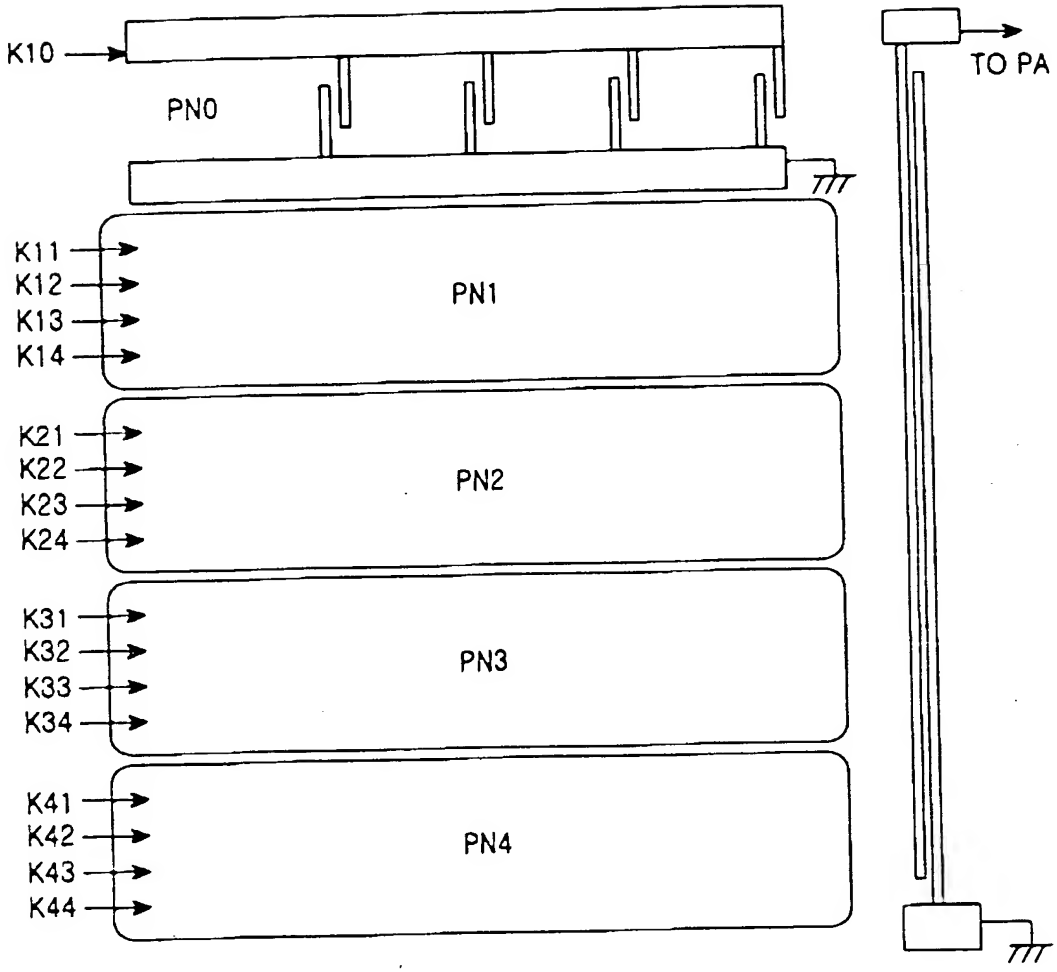
K10
PN0
TO PA
K11
K12
K13
K14
PN1
K21
K22
K23
K24
PN2
K31
K32
K33
K34
PN3
K41
K42
K43
K44
PN4

FIG.27

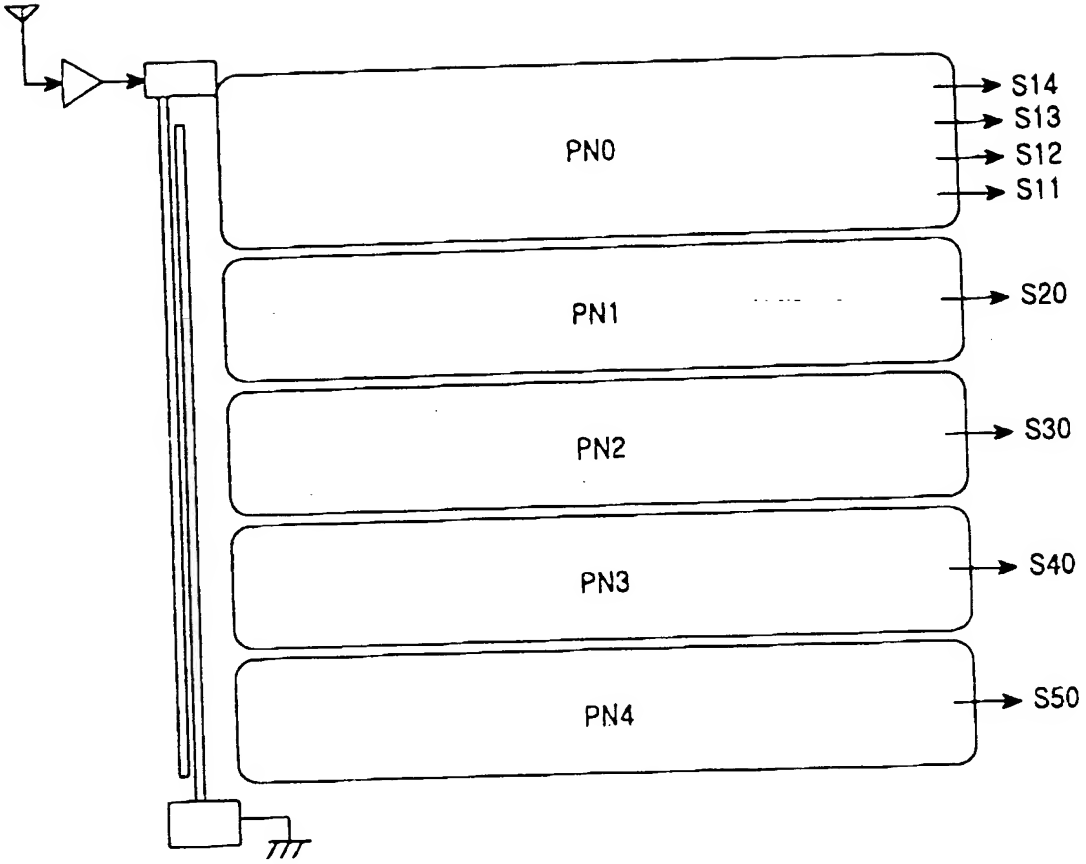

FIG.28

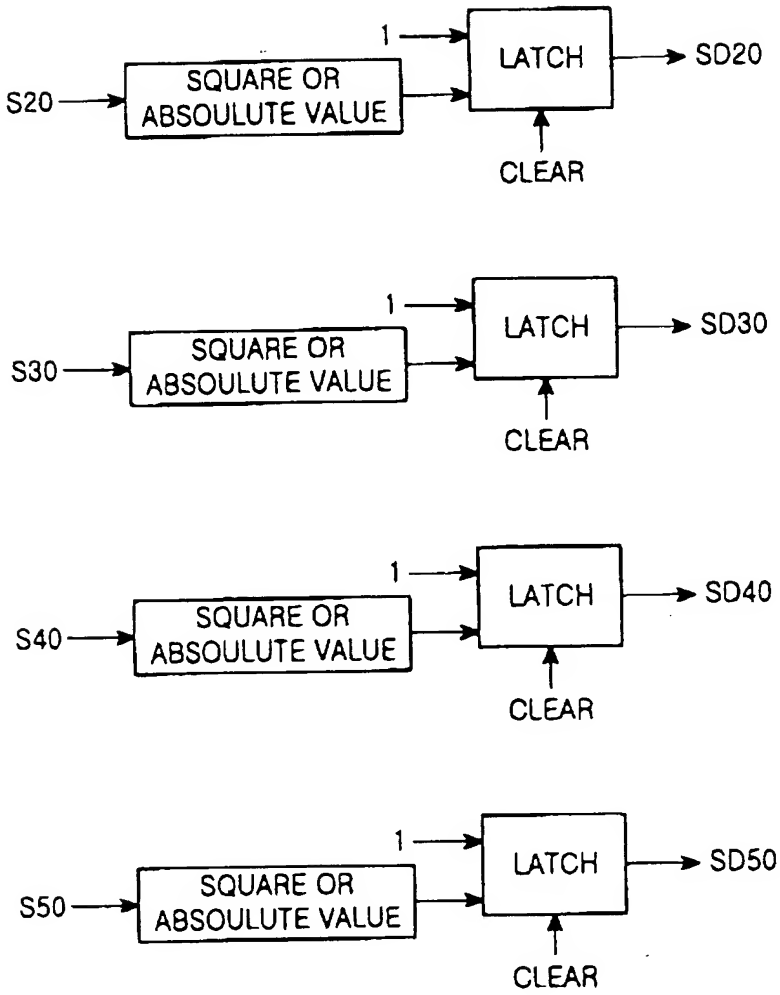
1
LATCH
SD20
S20
SQUARE OR
ABSOULUTE VALUE
CLEAR
1
LATCH
SD30
S30
SQUARE OR
ABSOULUTE VALUE
CLEAR
1
LATCH
SD40
S40
SQUARE OR
ABSOULUTE VALUE
CLEAR
1
LATCH
SD50
S50
SQUARE OR
ABSOULUTE VALUE
CLEAR

FIG.29

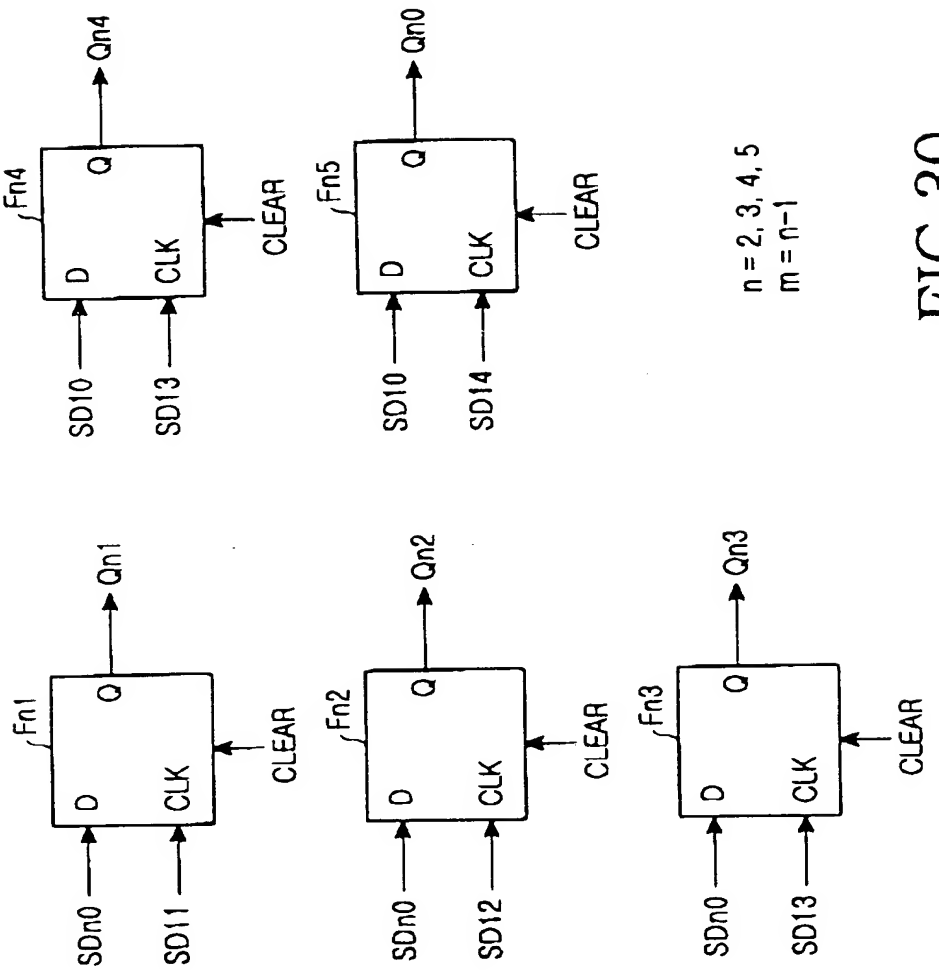
Fn4
Q
Qn4
D
CLK
CLEAR
SD10
SD13
Fn5
Q
Qn0
D
CLK
CLEAR
SD10
SD14
n = 2, 3, 4, 5
m = n-1
Fn1
Q
Qn1
D
CLK
CLEAR
SDn0
SD11
Fn2
Q
Qn2
D
CLK
CLEAR
SDn0
SD12
Fn3
Q
Qn3
D
CLK
CLEAR
SDn0
SD13

FIG.30

Qn0	Qn1	Qn2	Qn3	Qn4	DATA
1	0	1	1	1	0,0,i
1	0	0	1	1	0,1,i
1	0	0	0	1	1,1,i
1	0	0	0	0	1,1,i

i = n-2

FIG.31

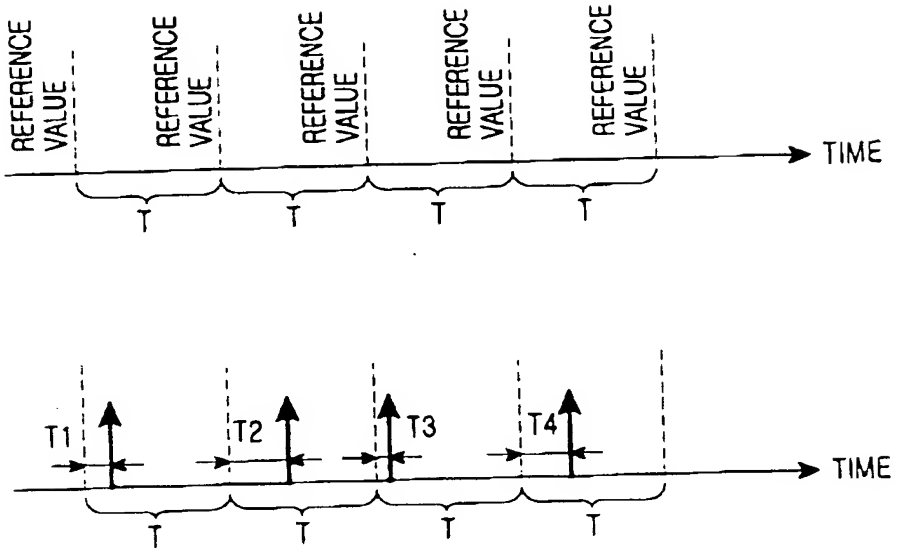

FIG.32

(PRIOR ART)

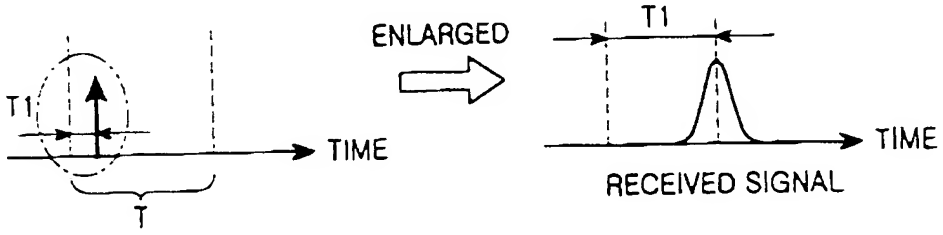

FIG.33

(PRIOR ART)

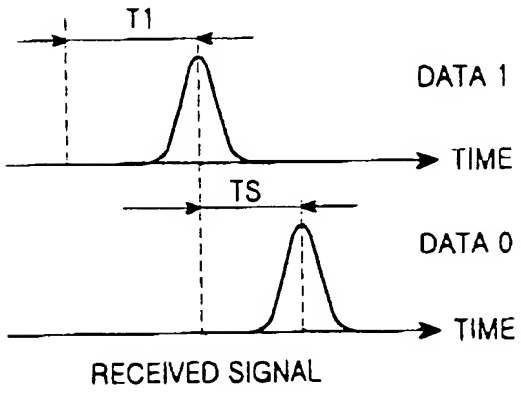

FIG.34

(PRIOR ART)

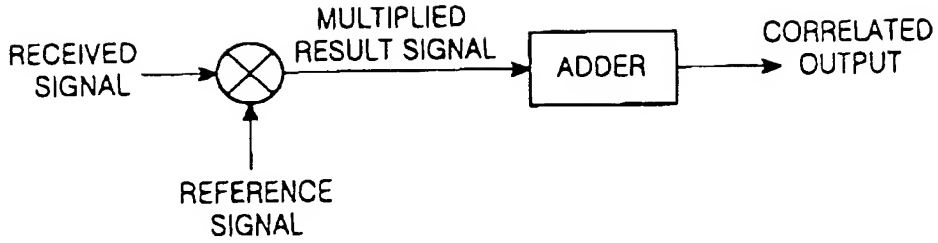

FIG.35

(PRIOR ART)

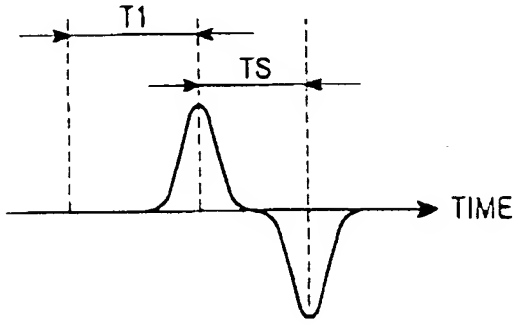

FIG.36

(PRIOR ART)

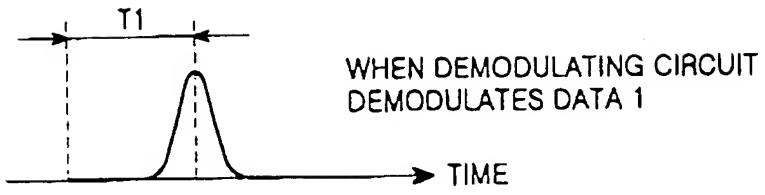

FIG.37

(PRIOR ART)

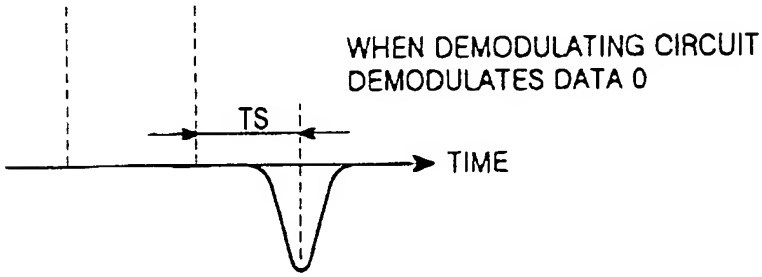

FIG.38

(PRIOR ART)

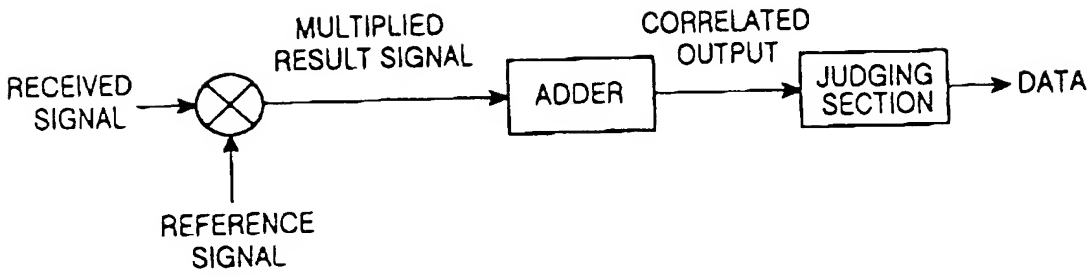

FIG.39

(PRIOR ART)

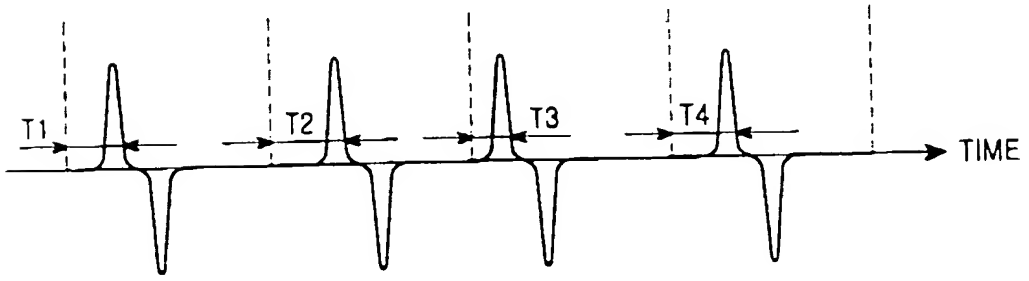

FIG.40

(PRIOR ART)

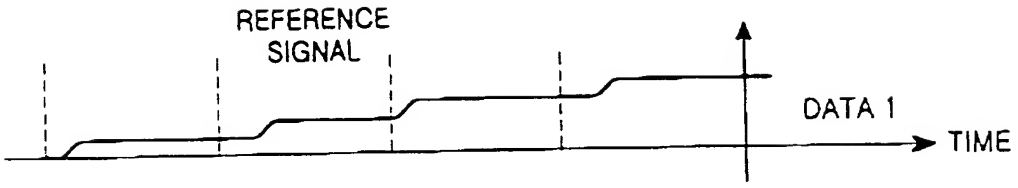

FIG.41
(PRIOR ART)

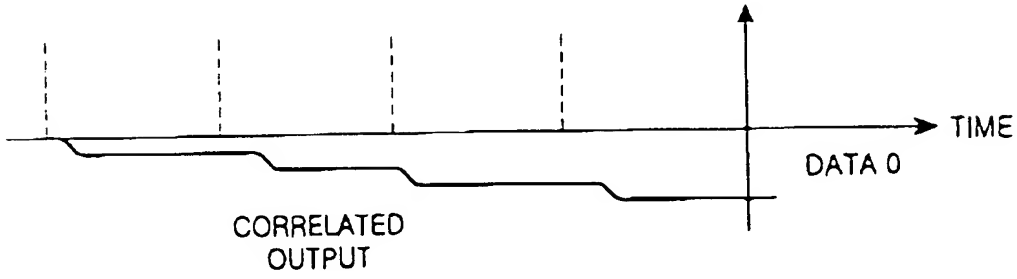

FIG.42
(PRIOR ART)

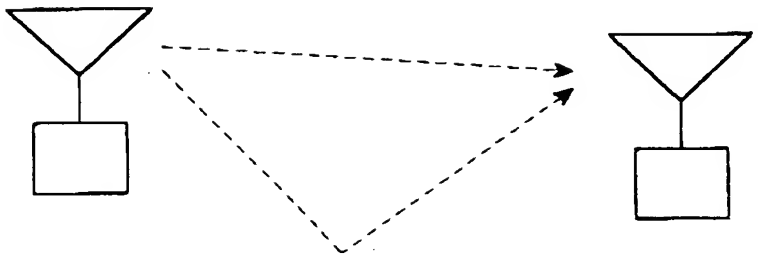

FIG.43

(PRIOR ART)

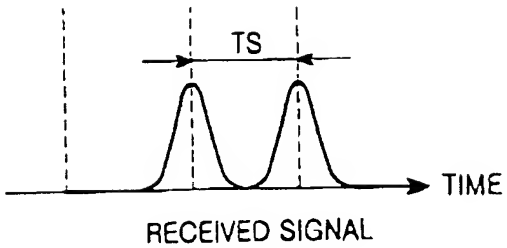

FIG.44

(PRIOR ART)

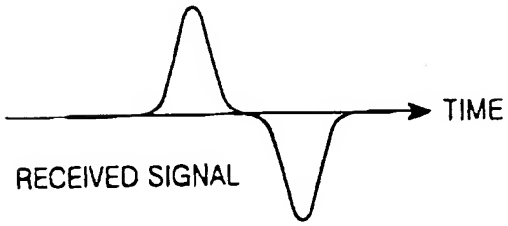

FIG.45

(PRIOR ART)